IN THE CLAIMS

Claims 1-33 (cancelled).

34. (currently amended) An intermediary of a semiconductor device comprising:

a semiconductor substrate formed with a first recessed region having a lower surface depressed with respect to a major surface of the semiconductor substrate;

a pillar region comprising a dielectric material formed in the first recessed region and extending from the lower surface, wherein a void region is formed within the pillar region; and

a polysilicon cap layer formed overlying all upper surfaces of the pillar region and ~~adjacent~~ aligned with the void region, wherein sidewall surfaces of the pillar region are devoid of the polysilicon cap layer, and wherein the pillar region, the polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

35. (previously presented) The intermediary of claim 34, wherein the polysilicon cap layer has a thickness of about 4,500 angstroms.

36. (previously presented) The intermediary of claim 34, wherein the upper surfaces of the pillar region are recessed below the major surface of the semiconductor substrate.

37. (previously presented) The intermediary of claim 36, wherein the upper surfaces are recessed a distance of about 0.5 microns.

38. (previously presented) The intermediary of claim 34, wherein the pillar region comprises deposited silicon dioxide.

39. (previously presented) The intermediary of claim 34, wherein the pillar region comprises a matrix of pillars.

40. (previously presented) The intermediary of claim 39, wherein at least a portion of the matrix of pillars includes pillars having a generally rectangular shape.

41. (previously presented) The intermediary of claim 34, wherein the pillar region comprises a contiguous matrix.

42. (previously presented) The intermediary of claim 34, wherein the pillar region extends a distance of about 4.5 micrometers from the lower surface and has a dielectric constant of about 3.5.